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ABSTRACT

A processor system having a cache memory. The replacement policy for the cache is augmented with a consideration of priority so that higher priority items are not  
5 displaced by lower priority items. The priority based replacement policy can be used to allow processes that are of lower priority to share the same cache with processes that are of higher priority. A processor including digital signal processing and general purpose logic function is shown to employ the priority based replacement policy to allow processes executing generalized logic functions to use the cache when not needed for  
10 digital signal processing operations that are time critical. A processor having digital signal processing capability is shown to employ the priority system to reserve a block of memory configured for a cache. The block of memory is reserved by setting the priority of those cache locations to a priority higher than any other executing process.